REMARKS

Summary of the Office Action

Claims 2, 3, 5, 6, 9, 10 and 12-15 are withdrawn from consideration.

Claims 1, 4, 7, 8 and 11 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,172,952 to Inokuchi et al. (hereinafter "Inokuchi").

Summary of the Response to the Office Action

The specification has been amended to correct several typographical errors.

Claims 1-13 remain as originally presented, and claims 14 and 15 remain as previously presented. Accordingly, claims 1-15 are pending, with claims 5, 6, 12 and 13 withdrawn from consideration.

Rejection under 35 U.S.C. § 102(b)

Independent claims 1, 7 and 8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Inokuchi. These rejections are respectfully traversed in view of the following comments.

With respect to the subject matter of independent claims 1, 7 and 8, it is respectfully submitted that Inokuchi fails to disclose each and every feature as claimed.

Inokuchi shows an optical disk device having a recording/reproduction section using a synchronization clock signal that is based on the wobble signal extracted from the optical disk. An abnormal jump is detected by monitoring a phase relationship between a frequency-divided signal of a synchronization clock signal, and a digitized wobble signal (*see* Inokuchi at column 11, lines 9-14).

In the Office Action, Inokuchi's gate signal generator 12 and frequency comparator 13, as shown in Fig. 1, are compared to the timing pulse generator recited in Applicant' claim 1. Inokuchi's frequency comparator 12 compares the frequency of a reference clock signal from a reference clock generator 11 with the frequency of a synchronization clock signal from a VCO 20 (*see* Inokuchi at column 10, lines 30-34). The gate signal generator 12 generates gate signals (*see* Inokuchi's Figs. 3E and 3F) using the synchronization clock signal from the VCO and

(*see* Inokuchi's Figs. 3E and 3F) using the synchronization clock signal from the VCO and provides the gate signal to various circuit blocks such as the demodulator 6. The operations of the demodulator 6 are described by Inokuchi at column 12, lines 55-57, and at column 13, lines 6-12. Demodulated address and demodulated data from the demodulator 6 are supplied to the error corrector/address detector 23, whose operations are described by Inokuchi at column 12, line 62, to column 13, line 5, and at column 13, lines 22-32.

Applicant's claims 1 and 7 recite combinations of features including "whereby the synchronization controller, in the case the corrected address data is determined as a correct address, then puts the synchronization process into stand-by for execution until the corrected address data is determined as an incorrect address" (emphasis added). Similarly, Applicant's claim 8 recites a combination of features including "whereby the synchronization control step, in the case the corrected address data is determined as a correct address, then puts the synchronization process into stand-by for execution until the corrected address data is determined as an incorrect address" (emphasis added).

Thus, according to the present invention, a "re-synchronism process" (*see* Applicant's specification as originally filed in the last line of page 1) is suspended until the corrected address data is detected to be defective.

According to one embodiment described in Applicant's specification as originally filed, the timing signal generation circuit 50 (details are shown in Fig. 3) includes a counter 501 receiving an initial value at its terminal DT and a sync detection signal SYC from the sync detection circuit 36 at its terminal LD. The timing signal generation circuit 50 also includes a counter 503 receiving a data load signal from an AND gate 504 and a signal based on a count value of the counter 501 through an adder 502. The details of the timing signal generation circuit 50 are described Applicant's specification as originally filed at, for example, page 16, line 10, to page 18, line 1. The control of the timing signal generation circuit 50 by the synchronization control circuit 40 is described in subsequent paragraphs.

In the flow of operations shown in Applicant's Fig. 4, once the synchronization control circuit 40 detects that the address data is correct (Error Zero signal E0=1, at step S44), the logical state of the synchronization command signal G1 is maintained '0' (the program proceeds through steps S44, S47, and S48, repeatedly in the normal address state ST2). In this state, the counter

503 in the timing signal generation circuit 50 operates in a self running mode, so that the "re-synchronism process" is suspended (typically described at, for example, page 24, lines 16-21). The normal address state ST2 is also depicted in Applicant's Fig. 5 and explained in the specification as originally filed at, for example, page 23, line 8, to page 24, line 15. Notably, the detection at step S44 (judgment of the Error Zero signal E0) is performed after the step S43 in which the synchronization command signal G1 is set to logic level '0' (synchronization is instructed when G1 is in logic level '1') is supplied to the timing signal generation circuit 50.

In contrast to the above-described features of claims 1, 7 and 8 of the present application, Inokuchi discloses that the reproduction signal is monitored, and a resynchronization process, in which the output signal of the gate signal generator 12 is shifted, is performed when a timing error of the reproduction signal is detected.

For at least any of the above reasons, it is respectfully submitted that the rejection under 35 U.S.C. § 102(b) of independent claims 1, 7 and 8 are improper and should be withdrawn, and that these claims are allowable over Inokuchi.

Claims 4 and 11 depended from independent claims 1 and 8, respectively, and thus recite the same allowable combination of features, as well as reciting additional features that further distinguish over Inokuchi. Accordingly, it is further respectfully submitted that the rejections under 35 U.S.C. § 102(b) of claims 4 and 11 are also improper and should be withdrawn.

Comments with respect to the Restriction Requirement

Reconsideration of the withdrawal of claims 2, 3 and 14 and claims 9, 10 and 15 is respectfully requested in view of the following comments.

When responding to the Election/Restriction Requirement dated July 7, 2006, Applicant elected the apparatus claims 1, 4, 7, 8, 11, 14 and 15 (specifies a: Fig. 4-5, first embodiment). Furthermore, the Applicant explained that claims 1 and 8 are generic to the elected species as well as to Species c (claims 2 and 9), Species d (claims 3 and 10), and species f (claims 14 and 15).

In the outstanding Office Action, claims 2, 3, 5, 6, 9, 10 and 12-15 stand withdrawn without traverse. However, as explained in the Response to Restriction/Election Requirement filed August 30, 2006, independent claims 1 and 8 are generic to species more than the elected

species a (Figs. 4-5). Furthermore, the independent claim 7 is directed to the species a (Figs. 4-5).

The following table explains the relationship between each of the apparatus claims 1-7 and the corresponding figures (the method claims are not included for purposes of simplicity.).

Claim 1	Figs. 4, 5
Claim 2	Figs. 8, 9
Claim 3	Figs. 10, 11
Claim 4	Figs. 4, 5
Claim 5	Figs. 6, 7 ... discussed below
Claim 6	Figs. 12, 13 ... discussed below
Claim 7	Figs. 4, 5
Claim 14	Figs. 14, 15

Among the embodiments shown in the groups of figures listed in the table, the loop marked "ADDRESS OK" associated with ST2 in Fig. 5 of the present invention, which is at least one of the features that distinguishes over the Inokuchi, also exists in the embodiments shown in Figs. 8 and 9, Figs. 10 and 11, and Figs. 14 and 15. Conversely, the two embodiments shown in Figs. 6, 7 and Figs. 12, 13, which respectively correspond to apparatus claims 5, 6 and method claims 12, 13, do not include the above-described feature.

Accordingly, it is respectfully submitted that only claims 5, 6, 12 and 13 are properly withdrawn from the present application, and that claims 2, 3, 9, 10, 14 and 15 depend, either directly or indirectly, from one of the allowable generic claims 1 and 8, and are therefore also allowable.

CONCLUSION

In view of the foregoing, Applicant submits that the pending claims are in condition for allowance, and respectfully request reconsideration and timely allowance of the pending claims. Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicant's undersigned representative to expedite prosecution. A favorable action is awaited.

EXCEPT for issue fees payable under 37 C.F.R. § 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due under 37 C.F.R. § 1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account No. 50-0573. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. § 1.136(a)(3).

Respectfully submitted,

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Dated: June 14, 2007

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